WHAT IS CLAIMED IS:

1. A process for forming a pattern comprising:

a resist pattern formation step of coating a first resist film and a second resist film in order on a film to be etched on a substrate, and further, forming a resist pattern by patterning said first resist film and said second resist film to make said first resist film broader than said second resist film while making said second resist film positioned on said first resist film;

a first patterning step of etching said film to be etched to form a first pattern in said film to be etched by using said resist pattern as a mask; and

a resist etching step of etching said resist pattern to remove remaining resist pattern at least a portion of said first resist film, said portion being not covered by said the second resist film, to thereby form a remaining resist pattern consisting of said first resist film and said second resist film, said resist etching step further being constructed such that said second resist film is in a state of a resist film having higher resistance against dry-etching than that of said first resist film at least during said resist etching step.

2. The process for forming a pattern according to claim 1, wherein said resist pattern includes a first opening formed in said first resist film and a second opening formed in said second resist film in said resist pattern formation step, said first opening is formed inside said second opening, and said remaining resist pattern is formed to have an overhang of said

second resist film with respect to said first resist film in said resist etching step.

3. The process for forming a pattern according to claim 1, wherein said second resist film is coated as a resist film having higher resistance against an etchant used in said resist etching step than that of said first resist film in said resist pattern formation step of coating said first resist film and said second resist film.

4. The process for forming a pattern according to claim 1, wherein said resist pattern is subjected to a plasma treatment step to modify said second resist film using a plasma treatment gas to change said second resist film into a modified resist film having higher resistance against dry-etching than that of said first resist film between said first patterning step and said resist etching step.

5. The process for forming a pattern according to claim 4, wherein said plasma treatment step employs one of a gas containing an O_2 gas, a gas containing a fluorine series gas and a gas containing a mixture of an O_2 gas and a fluorine series gas, as said plasma treatment gas.

6. The process for forming a pattern according to claim 4, wherein said resist etching step is further constructed such that said second resist film is made to include silicon atoms to change said second resist film into a silicon-doped second resist film and then, said silicon-doped second resist film is modified to a silicon oxide film through said plasma treatment step using a mixed gas containing at least oxygen.

7. The process for forming a pattern according to claim 6, wherein said second resist film previously consists of a resist film capable of being silylated and between said first patterning step and said plasma treatment step, a silylating step of immersing said first resist film and said second resist film in a silylating agent containing silazane to silylate only said second resist film is carried out.

8. The process for forming a pattern according to claim 1, wherein said second resist film is modified to a modified resist film having higher resistance against dry-etching than that of said first resist film, while removing at least a portion of said first resist film, said portion being not covered by said second resist film, in said resist etching step.

9. The process for forming a pattern according to claim 1, wherein a second patterning step of etching said film to be etched to form a second pattern in said film to be etched is carried out by using said remaining resist pattern as a mask after said resist etching step.

10. The process for forming a pattern according to claim 1, wherein a gate wiring and a gate insulating film covering said gate wiring are formed on said substrate and under said film to be etched, said film to be etched is a laminated film formed by depositing a semiconductor film, a semiconductor film doped with impurities and a metal film for source/drain electrodes in order on said gate insulating film, and said resist pattern is formed on said laminated film.

11. The process for forming a pattern according to claim 10, wherein said resist pattern is formed such that a resist

film out of said resist pattern, said resist film consisting of only said first resist film, is positioned above a later-formed channel region of a thin film transistor, at least said metal film for source/drain electrodes is etched and removed to form an electrode pattern made of said metal film for source/drain electrodes in said step of subjecting said film to be etched to said first patterning step by using said resist pattern as a mask, said resist pattern is etched to remove only said resist film consisting of only said first resist film to make said resist pattern become said remaining resist pattern in said resist etching step, and after said resist etching step, a second patterning step of etching and removing said metal film for source/drain electrodes, said semiconductor film doped with impurities and a part of said semiconductor film by using said remaining resist pattern as a mask to form a channel region of said thin film transistor in said laminated film is performed.

12. The process for forming a pattern according to claim 10, wherein a common electrode is formed together with said gate wiring to have comb-shaped electrodes and in said resist pattern formation step, said resist pattern consisting of said first resist film and said second resist film is formed on said metal film for source/drain electrodes to cover a later-formed pixel electrode, said later-formed pixel electrode being interposed between said comb-shaped electrodes of said common electrode.

13. The process for forming a pattern according to claim 10, wherein said second resist film is coated as a resist film having higher resistance against an etchant used in said resist

etching step than that of said first resist film in said resist pattern formation step.

14. The process for forming a pattern according to claim 11, wherein a plasma treatment step of modifying remaining resist pattern said second resist film out of said resist pattern to a modified resist film having higher resistance against dry-etching than that of said first resist film is performed between said first patterning step and said resist etching step.

15. The process for forming a pattern according to claim 14, wherein said modified resist film is formed such that said second resist film is made to include silicon atoms to change said second resist film into a silicon-doped second resist film and then, said silicon-doped second resist film is modified to a silicon oxide film through said plasma treatment step performed using a mixed gas containing at least oxygen.

16. The process for forming a pattern according to claim 11, wherein said process for forming a pattern further comprises after said second patterning step:

a step of removing said remaining resist pattern used to form said channel region of said thin film transistor and subsequently, depositing a protective insulating film covering said gate insulating film;

a step of coating a third resist film and a fourth resist film in order on said protective insulating film and patterning said third resist film and said fourth resist film to make said third resist film broader than said fourth resist film while making said fourth resist film positioned on said third resist film to form a second resist pattern consisting of said third

resist film and said fourth resist film, said second resist pattern having an opening therein;

a step of at least removing associated portion of said protective insulating film by using said second resist pattern as a mask to expose a surface of an electrically conductive layer consisting of said laminated film and positioned under said protective insulating film; and

a step of selectively etching said third resist film out of said second resist pattern to make an overhang of said fourth resist film with respect to said third resist film in said opening,

wherein said overhang is formed such that said fourth resist film is made to include silicon atoms to change said fourth resist film into a silicon-doped fourth resist film and then, said silicon-doped fourth resist film is modified to a silicon oxide film through a plasma treatment performed using a mixed gas containing at least oxygen, and thereafter, an associated part of said third resist film is removed in a lateral direction.

17. The process for forming a pattern according to claim 16, wherein an electrically conductive material is deposited on a surface consisting of said second resist pattern, said protective insulating film and said electrically conductive layer, and said second resist pattern is removed together with said electrically conductive material thereon to leave said electrically conductive material in and around said opening after forming said overhang.